IPFA 2021 Virtual Conference
Technical Program 14 September - 13 October 2021

Time, SGT (GMT + 0800hrs)	Plenary Session 14 September, Tuesday	
09:00 - 09:15 hrs	**Opening Address by General Chair - Nagarajan Raghavan, Singapore University of Technology & Design, Singapore**	
09:15 - 09:20 hrs	**Technical Program Briefing by TPC Chair - Alfred Quah, GlobalFoundries, Singapore**	
09:20 - 09:30 hrs	**BREAK (Connect to KN1 Live Session)**	
09:30 hrs	**Live Keynote Sessions (KN 1 - KN 3)**	
09:30 - 10:30 hrs	**KN 1** Session Chair : Nagarajan Raghavan	**Anomalous Mechanical Deformation – New Variable in Reliability for Flexible and Stretchable CMOS Electronics** *Speaker - Professor Muhammad Mustafa Hussain,* *UC Berkeley, USA*
10:30 - 10:40 hrs	**BREAK (Connect to KN2 Live Session)**	
10:40 - 11:40 hrs	**KN 2** Session Chair : Alfred Quah	**Reliability Insights from 25 Million Fully Autonomous Miles** *Speaker - Noah Lassar* *Waymo, USA*
11:40 - 11:50 hrs	Session Chair : Alfred Quah	**EDFAS FA Technology Roadmap Overview** *Speaker - Vinod Narang* *Advanced Micro Devices, Singapore*
11:50 - 13:00 hrs	**Lunch BREAK (Connect to KN3 Live Session)**	
13:00 - 14:00 hrs	**KN 3** Session Chair : Samuel Chef	**What's wrong with my chip? – Dr. AI, can you please diagnose?** *Speaker - Professor Aaron Thean* *National University of Singapore, Singapore*
14:00 - 14:10 hrs	**BREAK**	
14:10 hrs	**Best Paper Exchange Session (Pre-Recorded Video Presentations)**	
14:10 - 14:30 hrs	ISTFA 2020 Exchange Paper	**Quantum Diamond Microscope: Integrated Circuit Magnetic Field Imaging** *Dr. Edlyn V. Levine* *The MITRE Coporation* *Harvard University* *University of Maryland*
14:40 - 15:00 hrs	ESREF 2020 Exchange Paper	**FEM Simulation-Based Failure Analysis of Additive Manufacturing Liquid Cold Plates for More Reliable Power Press-Pack Assemblies** *Davide Spaggiari [1], Nicola Delmonte [1], Danilo Santoro [1], Federico Portesine [2], Filippo Vaccaro [2], Emilio Sacchi [2], Paolo Cova [1]* *[1] University of Parma, Italy, [2] POSEICO S.p.A, Italy*
End of Live Day		

Tutorials Session 14 September - 13 October 2021 (Video On Demand)			
FA Tutorials		**Reliability Tutorials**	
FA 1	**Scanning Probe Microscopies for Correlative Analysis of Advanced Technology Nodes** *Dr. Umberto Celano* *IMEC, Belgium* *MESA+ Institute for Nanotechnology, University of Twente, Netherlands*	**REL 1**	**Robust and Reliable Design for In-Memory Computing** *Prof Tuo-Hung Hou* *National Yang Ming Chiao Tung University,Taiwan*
FA 2	**Faster Fault Isolation with Advanced Data Analysis and Computer Vision** *Dr. Franco Stellari* *IBM T.J. Watson Reseach Center, USA*	**REL 2**	**Automotive Reliability Requirements & Challenges for Semiconductor Foundries** *Dr Oliver Aubel* *GlobalFoundries, Germany*

FA 3	**Contactless Fault Isolation Techniques and IC Hardware Security** *Prof Christian Boit* *TU Berlin, Germany*	**REL 3**	**3D IC Process Technology – Drivers, Technology Platforms, Challenges & Solution** *Prof Tan Chuan Seng* *Nanyang Technological University, Singapore*
FA 4	**Introduction of TEM/STEM Techniques in Analyzing Nano Materials** *Dr Jong-Shing Bow* *Integrated Service Technology Group, Taiwan*	**REL 4**	**Laser Diodes: An Introductory Tutorial** *Prof Massimo Vanzi* *University of Cagliari, Italy*

Track A - Emerging Topics in Failure Analysis & Reliability
14 September - 13 October 2021 (Video On Demand)

Invited	**Evaluation of Breakdown Interference and Strategy of Mitigating Yield Loss in Crossbar Memory Arrays** *Dr. I-Ting Wang - National Yang Ming Chiao Tung University, Taiwan*		
A1.1 (ID 16)	**Data analytics and Machine Learning: Root-Cause Problem-Solving Approach to prevent Yield Loss and Quality Issues in Semiconductor Industry for Automotive Applications** *Corinne Bergès [1], Jim Bird [2], Mehul D. Shroff [3], René Rongen [4], Chris Smith [3]* *[1] NXP, France, [2] NXP Chandler, USA, [3] NXP Austin, USA, [4] NXP Nijmegen, Netherlands*	**A1.5 (ID 74)**	**Reinforcement Learning to Reduce Failures in SOT-MRAM Switching** *Johannes Ender [1,2], Roberto Lacerda de Orio [2], Simone Fiorentini [1,2], Siegfried Selberherr [2], Wolfgang Goes [3], Viktor Sverdlov [1,2]* *[1] Christian Doppler Laboratory, [2] Institute for Microelectronics, TU Wien, Austria, [3] Silvaco Europe Ltd, United Kingdom*
A1.2 (ID 48)	**ASIC Circuit Netlist Recognition Using Graph Neural Network** *Xuenong Hong, Tong Lin, Yiqiong Shi, Bah Hwee Gwee* *Nanyang Technological University, Singapore*	**A1.6 (ID 93)**	**Extraction of Secrets from Allegedly Secret-free IoT Sensors using Artificial Intelligence** *Tuba Kiyan, Thilo Krachenfels, Elham Amini, Zarin Shakibaei, Christian Boit, Jean-Pierre Seifert* *TU Berlin, Germany*
A1.3 (ID 59)	**IC SynthLogo: A Synthetic Logo Image Dataset for Counterfeit and Recycled IC detection** *Mukhil Azhagan Mallaiyan Sathiaseelan, Manoj Yasaswi Vutukuru, Suryaprakash Vasudev Pandurangi, Shayan Taheri, Navid Asadizanjani* *University of Florida, USA*	**A1.7 (ID 94)**	**Failure Analysis of Large Area Pt/HfO2/Pt Capacitors Using Multilayer Perceptrons** *J. Muñoz-Gorriz [1], S. Monaghan [2], K. Cherkaoui [2], J. Suñé1, P.K. Hurley [2], E. Miranda [1]* *[1] Universitat Autònoma de Barcelona, Spain,* *[2] University College Cork, Ireland*
A1.4 (ID 62)	**Virtual Metrology of Visualizing Copper Microstructure Featured with Computer Vision and Artificial Neural Network** *Ling-Yen Yeh, Rencheng Chen* *Sun Innovation Co. Ltd, Taiwan*	**A1.8 (ID 101)**	**Generative Adversarial Network for Integrated Circuits Physical Assurance Using Scanning Electron Microscopy** *Md Mahfuz Al Hasan, Nidish Vashistha, Shayan Taheri, Mark Tehranipoor, and Navid Asadizanjani* *University of Florida, USA*
A1.9 (ID 123)	**Hybrid Modelling for the Failure Analysis of SiC Power Transistors on Time-Domain Reflectometry Data** *Simon Kamm, Kanuj Sharma, Ingmar Kallfass, Nasser Jazdi, Michael Weyrich* *University of Stuttgart, Germany*		

Track B - Metrology & Package Failure Analysis
14 September - 13 October 2021 (Video On Demand)

B1. Package Level Failure Analysis

Invited	**3D MIM Capacitor Embedded in TSV: Concept, Device Demonstration, Reliability and Applications** *Prof. Tan Chuan Seng - Nanyang Technological University, Singapore*		
B1.1 (ID 9)	**Atmospheric Corrosion of Ag/Cu Plated FeNi Based Leadframe used in MOSFET Package** *Lois Jinzhi Liao [1], Bisheng Wang [2], Juanlu Cai [2], Tao Zhang [3], Jing Liu [4], Liu Binhai [1], Xi Zhang [1], Younan Hua [1], Xiaomin Li [1]* *[1] WinTech Nano-Technology Services, Singapore* *[2] Huawei Technologies, China, [3] Northeastern University, China,* *[4] Wuhan University of Technology,China*	**B1.4 (ID 91)**	**Mechanical BEoL Stability Investigation at Cu-Pillars under Cyclic Load** *Jendrik Silomon [1], Jürgen Gluch [2], André Clausner [2], Ehrenfried Zschech [2]* *[1] Volkswagen AG, Germany,* *[2] Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany*
B1.2 (ID 30)	**Simple Methods to Improve the CSAM Thru-Scan Efficiency on Package Units** *Hao Tan, Hnin Hnin Win Thoung, Krishnanunni Menon, Htin Kyaw, Naiyun Xu, Pik Kee Tan, Changqing Chen* *GlobalFoundries, Singapore*	**B1.5 (ID 95)**	**A New 3D X-ray Solution for Non-Destructive Construction Analysis of Advanced Electronics Packages** *Yanjing Yang [1], Allen Gu [2], Thom Gregorich [3], Masako Terada [2]* *[1] Carl Zeiss X-ray Microscopy Applictations, Singapore* *[2] Carl Zeiss Research Microscopy Solutions, USA* *[3] Carl Zeiss Semiconductor Manufacturing Technology, USA*

B1.3 (ID 66)	**Failure Analysis on Diode-Triggered Silicon-Controlled Rectifiers By using Nondestructive X-ray Microscopy** *Xinqian Chen [1], Mengge Jin [1], Feihou [3], Fang Liang [1], Zijian Zhang [1], Yanan Wang [1], Dongming Liu [1], Le Chen2 Chaolun Wang [1], Zhiwei Liu [2], Xing Wu [1]* *[1] East China Normal University, China, [2] University of Electronic Science and Technology of China, China, [3] Chengdu University, China*	**B1.6 (ID 107)**	**A Systematic Failure Analysis Approach on Copper Pad Discoloration Issue** *Hemalatha Somu, Krishnan Arul* *Infineon Technology (Kulim) Sdn. Bhd, Malaysia*
B1.7 (ID 118)	**Digital Twin Aided IC Packaging Structure Analysis for High-quality Sample Preparation** *Chengjie Xi, Aslam A. Khan, John True, Nidish Vashistha, Nathan Jessurun, Dr. Navid Asadizanjani* *University of Florida, USA*		
B2. Sample Preparation, Metrology & Defect Characterization			
B2.1 (ID 20)	**SIMS Analysis of Ultra-Shallow Boron Implant** *Han Wei Teo, Yun Wang, Kenny Ong, Zhi Qiang Mo* *GlobalFoundries, Singapore*	**B2.7 (ID 57)**	**New Routine to Determine Microstructures of Metallic Interconnectors Using SEM-EBSD Technique** *Jiang Wu and Eugene Choo* *Oxford Instruments, Singapore*
B2.2 (ID 21)	**Sample Preparation For VCSEL Device Contamination Analysis** *Lei Zhu, Derrick Tan, Caryn Sek, Binghai Liu, Younan Hua, Xiaomin Li* *WinTech Nano-Technology Services , Singapore*	**B2.8 (ID 68)**	**Super wide area cross sectioning using broad Ar ion beam on solder bumping** *Natsuko Asano, Tamae Omoto, Lu Jinfeng, Shogo Kataoka, Shunsuke Asahina* *JEOL, Japan*
B2.3 (ID 24)	**A Novel CMOS Image Sensor Package Cover Glass White Stain Material Identification Metrology by TOF-SIMS** *Yeh Yee Kee, Kei Lin Sek, Lei Zhu, Younan Hua, Xiaomin Li* *WinTech Nano-Technology Services , Singapore*	**B2.9 (ID 69)**	**SIMS Methodology Study of Indium Implant Quantification** *Yun Wang, Kian Kok Ong, Han Wei Teo, Ramesh Rao Nistala and Zhi Qiang Mo* *GlobalFoundries, Singapore*
B2.4 (ID 35)	**The Monitor and Management of Sulfide Contamination for Probing FAB clean room** *Frank Su, W.F. Hsieh, Henry Lin, Vincent Chen, Y.S. Lou* *Ardentec Corporation, Taiwan*	**B.2.10 (ID 85)**	**TEM-EDX Characterization of Immersion Pd & Pd-MoOx on Cu & NiP** *Wan Tatt Wai, Arul Krishnan* *Infineon Technologies Sdn Bhd, Malaysia*
B2.5 (ID 40)	**X-ray Microanalysis Background Noise Reduction by FIB sample Preparation** *Kim Hong Yip, Poh Chuan Ang, Kwai Fun Lee, Ley Hong Khoo* *GlobalFoundries, Singapore*	**B2.11 (ID 99)**	**Automatic Defect Review of a Patterned Wafer using Hybrid Metrology** *Byung Woon Ahn, Ahjin Jo, Jubok.lee, Sang-Joon Cho* *Park Systems Corp, South Korea*
B2.6 (ID 52)	**Principal Component Analysis (PCA) of Surface Contamination by TOF-SIMS** *Kei Lin Sek, Pei Lin Lee, Khin Yin Pang, Younan Hua, Lei Zhu, Xiaomin Li* *WinTech Nano-Technology Services , Singapore*	**B2.12 (ID 100)**	**Guidelines of Plasma-FIB Delayering techniques for Advanced Process Node** *Ching-Chun Lin, Yun-Da Li, Kim Hsu* *Integrated Service Technology Inc., Taiwan*
B2.13 (ID 136)	**Simultaneous, Submicron Infrared and Raman Microspectroscopies for Effective Failure and Contamination Analyses** *Michael Lo [1], Mustafa Kansiz [1], Eoghan Dillon [1] Jay Anderson [1] Curtis Marcott [2]* *[1] Photothermal Spectroscopy Corp., USA, [2] Light Light Solutions LLC, USA*		

Track C - Electrical Fault Isolation & Product Diagnostic **14 September - 13 October 2021 (Video On Demand)**			
C1. Advanced Electrical Fault Isolation Techniques and Case Studies			
Invited	**Tool Automation and Computer Vision Methodologies for Faster IC Diagnostics** *Franco Stellari, Chung-Ching Lin, Fei Lan and Peilin Song - IBM, USA*		
Invited	**Logic State Imaging - From FA Techniques for Special Applications to One of the Most Powerful Hardware Security Side-Channel Threats** *Prof. Christian Boit - TU Berlin, Germany*		
C1.1 (ID 78)	**Low-Voltage EBIC Investigation of Fails** *Andreas Rummel [1], Greg M. Johnson [2], Matthias Kemmler [1], Thomas Rodgers [3]* *[1] Kleindiek Nanotechnik, Germany, [2] Zeiss Microscopy, USA, [3] Zeiss Microscopy, Germany*	**C1.5 (ID 44)**	**MIPI RFFE Functional Leakage Failure Debug using an Integrated NI-PXIe Setup** *D. Nagalingam, A.C.T. Quah, S.J. Moon, J.C. Alag, A.W. Teo* *GlobalFoundries, Singapore*

C1.2 (ID 81)	**Proposal for Advanced Devices Analysis using 930nm Light Source and GaAs SIL** Tomonori Nakamura, Akihito Uchikado, Mitsunori Nishizawa, Ikuo Arata, Masanori Kobayashi, Xiangguang Mao, Akira Shimase Hamamatsu Photonick K.K., Japan	**C1.6 (ID 67)**	**Finding Invisible Cracks via Nano-Probing** Lai-Seng Yeoh [1], Kok-Cheng Chong [1], Susan Li [2], Andreas Rummel [3] [1] Infineon Technologies Memory Solutions Malaysia Sdn. Bhd, Malaysia, [2] Infineon Technologies Inc., USA, [3] Kleindiek Nanotechnik GmbH, Germany
C1.3 (ID 92)	**Meticulous System Calibration as a key for extracting correct Photon Emission Spectra** Norbert Herfurth [2], Christian Boit [1] [1] Berlin University of Technology, Germany, [2] IHP – Leibniz-Institut für innovative Mikroelektronik, Germany	**C1.7 (ID 90)**	**Case Studies: Masked Read-Only Memory Failure Fault Isolation without Bitmapping** BL Yeoh, MH Thor, LS Gan, SH Goh, YH Chan, WF Soh,C. Shaalini, Wiswa Naradha GlobalFoundries, Singapore
C1.4 (ID 33)	**Dynamic Defect Localization by Toggling Integrated Circuits States** Ke-Ying Lin, Paul Kenneth Ang, Chun-Wei Ke, Toby Chen NXP Semiconductors, Taiwan	**C1.8 (ID 98)**	**Significance of Dynamic Electrical Fault Isolation Techniques on Buried Via Void defects** MH Thor, SH Goh, BL Yeoh, LS Gan, YH Chan GlobalFoundries, Singapore
C2 Product Test and Diagnostics			
Invited	**Localization of Front-end Defects Using Volume Scan Diagnosis** Jayant D'Souza - Siemens EDA, USA		
C2.1 (ID 54)	**Hysteresis Effect Induces the Inductor Power Loss of Converter during the Voltage Conversion** Jian-Hsing Lee [1], Karuna Nidhi [1], Chung-Yu Hung [2], Ting-Wei Liao [2], Wu-Yang Liu [2], Hung-Der Su [2] [1] Vanguard International Semiconductor Corp, Taiwan [2] Richtek Technology Corporation, Taiwan	**C2.3 (ID 124)**	**E-test Probe Mark Topology-induced Failure** JF Jong [1], TW Lim [1], SH Goh [1], Yang Qu [2], Jeffrey Lam [2] [1] Globalfoundries Singapore [2] Star-Quest Technologies Singapore
C2.2 (ID 111)	**Digital and AMS Yield Diagnosis Flow Combining Automated Testing and Fault Injection-based Circuit Simulation** C. Shaalini [1], Song li [1], SH Goh [1], WF Soh [1], GlobalFoundries, Singapore	**C2.4 (ID 125)**	**Failure Analysis of a PROM at Low Temperature Induced by Process Deviation** Pengfei Lian [1], Jianshe Lou [1], Yunlong Liu [2], Peipei Fan [1], Rong Zhao [1], Zebin Kong [1], Weiming Zhu [1], Kunshu Wang [1], Lu Tang [3] [1] Institute of Shanghai Academy of Spaceflight Technology, China, [2] Shenzhen State Microelectronics Co., China, [3] University of Shanghai for Science and Technology, China

Track D - Physical Failure Analysis **14 September - 13 October 2021 (Video On Demand)**			
D1. Advanced Physical Failure Analysis Techniques			
Invited	**Dielectric Breakdown in Hexagonal Boron Nitride** Dr. Alok Ranjan - Singapore University of Technology & Design, Singapore		
D1.1 (ID 13)	**Investigation on the Copper Void Defect by Transmission Electron Microscope (TEM)** Chi Wen Soo, Jie Zhu GlobalFoundries, Singapore	**D1.5 (ID 65)**	**Local Capacitance-Voltage Profiling and Deep Level Transient Spectroscopy of SiO2/SiC Interfaces by Scanning Nonlinear Dielectric Microscopy** Kohei Yamasue, Yasuo Cho Tohoku University, Japan
D1.2 (ID 22)	**Silicon Defect Observation From Ultra-Thick Sample Using TEM EELS Technique** Gek Li Lee, Kok Wah Lee, Jie Zhu GlobalFoundries, Singapore	**D1.6 (ID 103)**	**Improving Tomographic Sensing of Scalpel SPM with Multi-Probe Functionality and Automatic Removal Rate Extraction** C. O'Sullivan [1], M. Tedaldi [1], C. Drilakis [2], T. Hantschel [2], A.D.L. Humphris [1,3], J.P.Hole [1], J. Goulden [1], U. Celano [2,4] [1] Infinitesima, United Kingdom, [2] IMEC, Belgium, [3] University of Bristol, United Kingdom, [4] University of Twente, Netherlands
D1.3 (ID 38)	**TEM EELS Analysis for DRAM Failure Analysis** S. Y. Chen, W. Yang, G. F. Xu, C. T. Liu Changxin Memory Technologies, China	**D1.7 (ID 109)**	**Innovative use of TCAD Process Simulation for Device Failure Analysis** Shang Yi Lim, Joydeep Ghosh, Aaron Thean National University of Singapore, Singapore
D1.4 (ID 56)	**3D NAND Memory Auto-delayering with Generic Delayering Model Using PFIB** Bingxing Wu [1], Ruixin Zhang [1], Zhengqiang Guo [1], Zhenxin Zhong [2] [1] Thermo Fisher Scientific, China, [2] Thermo Fisher Scientific, USA		

D2. Case Studies on Physical Failure Analysis

Invited	**Direct Visualization of Breakdown Induced Metal Migration in ESD Devices** *Prof. Xing Wu - East China Normal University, China*		
D2.1 (ID 55)	**The Failure Mechansim of the E-SOA Boundary of Power Transistor Collapsed at Higher Gate Voltage** *Jian-Hsing Lee, Karuna Nidhi, Tingyou Lin, Hsueh-Chun Liao, Fu-Chun Tseng, Scott Lee* *Vanguard International Semiconductor Corp., Taiwan*	**D2.5 (ID 73)**	**Failure Analysis on MIM Capacitor Failures of RF Devices using Simple Circuit Edit Passive Voltage Contrast Method** *Siong Luong Ting, Pik Kee Tan, Naiyun Xu, Hnin Hnin Win Thoungh, Htin Kyaw, Krishnanunni Menon, Yanlin Pan, Hao Tan, Changqing Chen* *GlobalFoundries, Singapore*
D2.2 (ID 58)	**Reliability Analysis using Advanced Modeling Technique for MEMS Microphone** *Shubham Shubham, Xin Song, Yunfei Ma, Mark G. da Silva, Zhijun Guo, Jeremy Johnson, Michael Pedersen* *Knowles Corporation, USA*	**D2.6 (ID 76)**	**Application of Ion Chromatography in Corrosion Failure Analysis of Components and Devices** *Chao Cui[1], Yun Zhao[1], Yong Xiao[1], Ziwen Cai[1], Haolin Wang[1], Jin Li[2], Shengzong He[3]* *[1] Electric Power Research Institute of CSG, China* *[2] Honghe Power Supply Bureau, China* *[3] CEPREI Lab, China*
D2.3 (ID 60)	**Study on the Factors of Start-up White Line Caused by Coupled Electric Field in TFT LCD** *Xin Li, Yong Song , Hongjun Yu, Chuncheng Che, Hailin Xue* *BOE Optoelectronics Technology CO., China*	**D2.7 (ID 86)**	**The Influence of Adhesive Tape on L0 Light Leakage of TFT-LCD Products after Reliability Test** *Tianyu Xu[1], Gang Yang[1], Zheng Jia[1], Jingang Wang[1], Yong Song[1], Hongjun Yu[1], Chuncheng Che[1], Hailin Xue[2]* *[1] Beijing BOE Optoelectronics Technology Co., China,* *[2] BOE Technology Group Co., China*
D2.4 (ID 63)	**Metal Migration Induced Breakdown from Gate Contact in Bulk FinFET Devices** *Xin Yang[1], Yihong Qing[2], Kuei-Shu Chang-Liao[3], Yuchong Qiao[1], Chaolun Wang[1], Zhiwei Liu[2], Luoyong Li[4], Chihang Tsai[4], Yongren Wu[4], Yazhen Xie[4], Weisong Yu[4], Xing Wu[1]* *[1] East China Normal University, China, [2] University of Electronic Science and Technology of China, China, [3] National Tsing Hua University, Taiwan, [4] China Chinaisti (Shanghai) Testing Technology Co., China*	**D2.8 (ID 115)**	**Failure Analysis Techniques and Studies on Vertical Short Issue for Production Wafers** *P.K. Tan, S.L. Ting, Y.L. Pan, N.Y. Xu, D. Nagalingam, H.H.W. Thoungh, H. Kyaw, H. Tan, K. Menon, R. Fransiscus, A. Quah, P.T. Ng, S. M. Parab, C.Q. Chen.* *GlobalFoundries, Singapore*
D2.9 (ID 137)	**Analysis of a Failure in High-Voltage VDMOS Device caused by Die Contamination** *Zhaoxi Wu, Chao Duan, Zhiming Ding,Yaning Wu, Rui Cao, Xu Wang, Meng Meng* *China Aerospace Components Engineering Center, China*		

Track E - Devices, Interconnects & Packaging Reliability
14 September - 13 October 2021 (Video On Demand)

E1. Transistor and NVM Device Reliability

Invited	**Random Telegraph Noise for Advanced True Random Number Generation in the IoE ecosystem** *Dr. Francesco Puglisi - Università di Modena e Reggio Emilia, Italy*		
Invited	**Wafer-Scale Epitaxial 2D Transition Metal Dichalcogenides for High-Performance Scaled Transistors** *Dr. Yuanyuan Shi - IMEC, Belgium*		
E1.1 (ID 5)	**Analysis for the Physical Mechanism of the Abnormal Increase of Idsat in NMOS under HCI** *Wei-Cheng Chu, Bo-An Tsai, Cheng-Te. Chen, Chi-Li Chang, Wei-fong Lin* *Powerchip Semiconductor Manufacturing Corp., Taiwan*	**E1.7 (ID 97)**	**Pitfalls for the Characterization of Self-Heating Effect in Nano-Scaled Devices** *Dongxing Zhang, Pengpeng Ren, Zhigang Ji* *Shanghai Jiaotong University, China*
E1.2 (ID 6)	**Physical Mechanism for Different Phases and Turn-Around of Idsat in PMOS under HCI Stress** *Bo-An Tsai, Wei-Cheng Chu, Yu-Chih Chang, Yi-Heng Chen, Chien-Fu Chen* *Powerchip Semiconductor Manufacturing Corp., Taiwan*	**E1.8 (ID 102)**	**A Reliability-Concerned Compute-in-Memory Behavior Model for Convolutional Neural Network** *Kaili Cheng, Jiahao Song, Xinyue Zhang, Yandong He, Runsheng Wang, Yuan Wang* *Peking University, China*

E1.3 (ID 32)	**Influence of RPO Film and CESL Material on Data Retention in Non-Volatile Memory** Yen-Ting Chen, Ming-Shan Lo *eMemory Technology Inc., Taiwan*	**E1.9 (ID 104)**	**Comparison of DC/AC Hot Carrier Degradation between Short Channel Si Bulk and SiGe SOI p-FinFETs** Hao Chang[1,3], Yongkui Zhang[1,3], Longda Zhou[1,3], Zhigang Ji[2], Hong Yang[1,3], Qianqian Liu[1,3], Yongliang Li[1,3], Renrong Liang[4], Eddy Simoen[5], Huilong Zhu[1,3], Jun Luo[1,3], Wenwu Wang[1,3] *[1] Chinese Academy of Science, China, [2] Shanghai Jiaotong University, China, [3] University of Chinse Academy of Sciences, China, [4] Tsinghua University, China, [5] IMEC, Belgium*
E1.4 (ID 46)	**NAND Flash Relationship Between the Initial State of Non-Volatile Memory Cycling Endurance and the High Temperature Data Retention Ability of Post Cycling** Chia-Sheng Huang, Yun-Chi Liao *Powerchip Semiconductor Manufacturing Corp., Taiwan*	**E1.10 (ID 114)**	**Analysis of The Threshold Voltage Instability under Semi-ON Hot Electron Stress in AlGaN/GaN High Electron Mobility Transistor** Fong-Min Ciou[1], Yu-Shan Lin[1], Jia-Hong Lin[1], Ting-Tzu Kuo[1], Jui-Tse Hsu[2], Po-Hsun Chen[3], Ting-Chang Chang[1] *[1] National Sun Yat-sen University, Taiwan, [2] National Tsing Hua University, Taiwan, [3] R. O. C. Naval Academy, Taiwan,*
E1.5 (ID 72)	**A Comprehensive Negative Bias Temperature Instability Model for Gallium-nitride Metal-insulator-semiconductor High Electron Mobility Transistors From 77K to 393K** Ting-Tzu Kuo[1], Ying-Chung Chen[1], Yu-Shan Lin[1], Yu-Chieh Chien[2], Fong-Min Ciou[1], Po-Hsun Chen[3], and Ting-Chang Chang[1] *[1] National Sun Yat-sen University, Taiwan, [2] National University of Singapore, Singapore, [3] R. O. C. Naval Academy, Taiwan*	**E1.11 (ID 117)**	**Degradation Studies on 8-Layer 3D Vertical Resistive Random Access Memory Under Moisture** Dengyun Lei[1], Huiwei Wu[1], Yiqiang Chen[1], Yun Huang[1], Yunfei En[1], Qiantong Guo[2], Feng Zhang[3], Rui Gao[1] *[1] The No.5 Electronics Research Institute of the Ministry of Industry and Information Technology, China, [2] China Electronics Corporation, China, [3] Chinese Academy of Sciences, China*
E1.6 (ID 83)	**HCI SOA Enhancement for EDNMOS with Metal Field Plate** J.M. Soon, P.Y. Tan, C.W. Eng, M.Cai, M.Li *GlobalFoundries, Singapore*	**E1.12 (ID 133)**	**Study of Layout Effect on Gate Oxide TDDB in Sub-16nm FinFET Technology** Xiangyu Liu[1], Yongsheng Sun[1], Junlin Huang[1], Changze Liu[1], Xiaolu Shang[1] *Hisilicon Technologies Co., China*
E2. Interconnect and Packaging Reliability			
Invited	**BEOL Reliability Challenges in Advanced Nodes for Automotive Applications** *Dr Markus Herklotz - GlobalFoundries, Germany*		
E2.1 (ID 17)	**Failure Mechanism of Stress Migration in Via Sidewall for Dual Damascene Cu Interconnection** Yu Chun Teng, Liwei Yang *Powerchip Semiconductor Manufacturing Corp., Taiwan*	**E2.5 (ID 96)**	**Rapid Assessment of Semiconductor Thermal Quality** Voon Hon Wong[1], Andras Vass-Varnai[2], Antonio Caruso[3], Young Joon Cho[4], Yong Seoung Lee[4], Kwon Hyung Lee[4] *Siemens Digital Industry Software, [1] Singapore. [2] USA, [3] Italy, [4] Republic of Korea*
E2.2 (ID 37)	**Electromigration of Gold Metallization** Christine Hau-Riege, YouWen Yau *Qualcomm Technologies, Inc., USA*	**E2.6 (ID 108)**	**Temperature Cycling Failure Analysis and Improvement of A Panel Level Fan-out QFN Package** Li Chen[1], Wei Gao[1], Yan Huo[2], Lei Xie[2], Yuyu Peng[1], Min Ren[1], Bo Zhang[1] *[1] University of Electronic Science and Technology of China, China, [2] SiPLP Microelectronics(Chongqing) Co., China*
E2.3 (ID 88)	**In-situ SEM Micromechanical Experiments on Dual Damascene Copper Test Structures for Investigation of Interfacial Properties of Copper Interconnects** Wieland Heyn[1], Hanno Melzner[2], Klaus Goller[2], Sergey Ananiev[2], André Clausner[1], Johannes Zechner[3], Ehrenfried Zschech[1], *[1] Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany, [2] Infineon Technologies AG, Germany, [3] KAI Kompetenzzentrum Automobil- und Industrielektronik GmbH, Austria*	**E2.7 (ID 116)**	**Analytical and Finite Element Study on Warpage and Stress of 2.5D Chip-Package Structures** Sida Hao[1], Weishen Chu[1], Paul S. Ho[1], Joonsik Sohn Lee[2], Rui Huang[1] *[1] University of Texas, USA, [2] Samsung Electronics, S.Korea*
E2.4 (ID 89)	**Nano-CT Imaging of Electrically Stressed Power Device Metallization** Dominik Mueller[1], Christian Fella[2], Frank Altmann[3], Jonas Graetz[2], Andreas Balles[2], Matt Ring[4], Jeff Gambino[4] *[1] University of Würzburg, Germany, [2] Fraunhofer Development Center X-Ray Technology EZRT, Germany, [3] Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Germany, [4] ON Semiconductor, USA*	**E2.8 (ID 134)**	**Electromigration Failure Controlled by Aging-like Gradual Resistance Shift in Co-Capped Cu Interconnects** Hui Zheng, Yongsheng Sun, Weichun Luo, Junlin Huang *Hisilicon, China*

Track F - ESD/Latchup, Photonics & High Power Reliability
14 September - 13 October 2021 (Video On Demand)

F1. Photonics and High Power/Wide Bandgap Device Reliability and Failure Analysis

Invited	**Wave Aspects in Laser Diode Catastrophic Optical Damages** *Prof. Massimo Vanzi - University of Cagliari, Italy*		
Invited	**Reliability and Characterization of GeSe OTS Selector Device** *Prof. Weidong Zhang - Liverpool John Moores University, United Kingdom*		
F1.1 (ID 29)	**Research on the Design Factors Affecting the COG Mura of IPS Display Products** *Bao Yazhou, YANG Gang, JIA Xingge, SONG Yong, YU Hongjun, CHE Chuncheng, XUE Hailin* *Beijing BOE Optoelectronics Technology Co., China*	**F1.4 (ID 87)**	**Stability of Schottky Barrier Diode Integrated in p-GaN Enhancement-mode GaN Power Technology** *Jethro Oroceo Gallardo[1], Brice De Jaeger[2], Sachidananda Dash[1], Shun-Wei Tang[1], Thanh Nga Tran[1], Dirk Wellekens[2], Benoit Bakeroot[2,3], Stefaan Decoutere[2], and Tian-Li Wu[1]* *[1] National Yang Ming Chiao Tung University, Taiwan* *[2] IMEC, Belgium, [3] IMEC and Ghent University, Belgium*
F1.2 (ID 50)	**Analysis and Improvement of Repeated Wake-up Jittering H-line** *Qiang Wang, Zhengxin Zhang, Ye Wang, Honggui Jin,Qi Sun,Yong Song, Hongjun Yu, Hailin Xue, Chuncheng Che* *Beijing BOE Optoelectronics Technology Co., China*	**F1.5 (ID 110)**	**Failure Analyses and Reliability Improvement of the Corner Region of Variation Lateral Doping Termination** *Min Ren[1], Xuefan Zhang[1], Xin Zhang[2], Junwei Feng[1], Yahan Yang[1], Youke Bai[1], Jiakang Fan[1], Rongyao Ma[2], Fang Zheng[2], Yining Ma[1], Zehong Li[1], Bo Zhang[1]* *[1] University of Electronic Science and Technology of China, China,* *[2] Wuxi China Resources Huajing Microelectronics Co., China*
F1.3 (ID 71)	**Research on the Relationship between the Limit Design and Material of the LGP and the Damage of the LGP** *Wang Shixin[1], Yang Gang[1], Song Yong[1], Yu Hongjun[1], Che Chuncheng[1], Xue Hailin[1], Wang Kai[2]* *[1] Beijing BOE Optoelectronics Technology Co., China,* *[2] Beijing Digital Video Technology Co., China*	**F1.6 (ID 119)**	**Charge–Sensing method for Nickel Contamination Detection on a 4H-SiC PowerMOSFET** *B. Mazza[1,2], F. Cordiano[1], M. Boscaglia[1], V. Scuderi[1], M. Frazzica[1], R. Ricciari[1], M. Poma[1], C. Gagliano[1], S. Patanè[2]* *[1] STMicroelectronics, Italy,* *[2] Universita' degli Studi di Messina, Italy*

F2. ESD, Latchup and Reliability for Space Applications

Invited	**Latchup: From the Beginning to Today** *Dr. Stephen H Voldman - Voldman Consulting, USA*		
F2.1 (ID 14)	**Study on Transmitter with Stacking-MOS Structure of Interface Circuits for Cross-Domain CDM ESD Protection** *Cheng-Yun Hsueh, Ming-Dou Ker* *National Yang Ming Chiao Tung University, Taiwan*	**F2.3 (ID 53)**	**Analyze the ESD Performance and Bandwidth Difference for LC T-Network and Bridged T-Coil** *Jian-Hsing Lee[1], Karuna Nidhi [1], Natarajan Mahadeva Iyer[2]* *[1] Vanguard International Semiconductor Corp., Taiwan* *[2] Allegro Microsystems Inc., USA*
F2.2 (ID 27)	**Research on reducing electro-static discharge of tearing film of EPD** *Haowei Zou, Xin Li, Yong song, Hanqing Liu, Junru Ma, Hongjun Yu, Chuncheng Che, Hailin Xue* *BOE Optoelectronic Technology Co., China*	**F2.4 (ID 112)**	**HV ESD Device Solution Evaluations in 55nm BCD Technology** *Sagar P Karalkar[1], Milova Paul[1], Xiao Mei Elaine Low[1], Kyong Jin Hwang[1], Robert Gauthier Jr[2]* *[1] GlobalFoundries, Singapore* *[2] GlobalFoundries, USA*
F2.5 (ID 126)	**Electrostatic Discharge Switch Simulation Enablement in RF SOI Technologies** *Mengfu Di, Anindya Nath, Meng Miao, XiangXiang Lu, Lin Lin, Robert Gauthier* *GlobalFoundries Corporation, USA*		

Note : IPFA 2021 Technical Program is tentative and subjected to changes